EXHIBIT 8

RM-9460
GRAPHIC DISPLAY SYSTEM
Hardware Reference Manual

Publication No. 8000080-01, Revision A

September 1982

AX209970

Ramtek

2211 Lawson Lane
Santa Clara, California 95050

LIST OF EFFECTIVE PAGES

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Chapter 1

GENERAL INFORMATION

1.1 INTRODUCTION

The 9460 product line is designed and manufactured by Ramtek Corporation, 2211 Lawson Lane, Santa Clara, California 95050. This hardware reference manual provides a qualified technician with all the information necessary to install, configure, operate, and maintain the 9460.

1.2 HOW TO USE THIS MANUAL

This manual is a single volume reference for the 9460 operator or technician. Chapter divisions are as follows:

- Chapter 1 - General Information
- Chapter 2 - Installation
- Chapter 3 - Operation
- Chapter 4 - Functional Description
- Chapter 5 - Maintenance
- Chapter 6 - Parts List
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- Index

1.2.1 General Information

Chapter 1 gives an overview of the manual, a summary of related documents, safety precautions and warnings, Ramtek service information, and a detailed equipment description.

1.2.2 Installation

Chapter 2 contains receiving and reshipping information and detailed facility requirements. System configuration, turn-on, checkout, and expansion are included.

1.2.3 Operation

Chapter 3 describes and locates 9460 terminal controls and indicators. Instructions include turn-on, operation, and turnoff.

4.4 9460 FUNCTIONAL DESCRIPTION

A typical 9460 (figure FO4-1) has 8 functional elements:

- (Z80) system processor PCB or (68000) system processor PCB
- Sync PCB
- Serial link PCB
- Memory control processor PCB
- 10X12 memory PCB
- Video 7 PCB
- Backplane
- Power Supplies

The system processor PCB controls terminal operation, decodes instructions from the host and drives the MCP.

The sync PCB is the source of system clocks and generates synchronizing signals which drive a CRT monitor and related 9460 logic which must be synchronized with raster scans as they occur in the monitor. This PCB also has a TTL DMA sequencer, reset logic for the 9460 a cursor pattern generator (one cursor), and terminations for the memory timing signals.

The serial link PCB processes operator input from serial transmission peripheral devices and has a cursor generator which can generate four cursors.

The memory control processor (MCP) PCB controls display operations associated with the 10X12 memory PCB. Screen refresh and memory refresh are carried out under control of this PCB. In addition the MCP draws primitives such as alphanumerics, graphics, and images and performs clipping, entity detection, pan and zoom.

The 10X12 memory PCB incorporates 64K MOS RAMs that store picture information in raster scan, dot matrix format. Memory is organized into 8 memory planes.

The video 7 PCB accepts digital video data from the 10X12 memory PCB and outputs analog RGB signals to a video monitor. This PCB has a video lookup table that stores values loaded from the processor. Stored VLT data generates intensity values for the digital- to-analog converter (DAC) when addressed by refresh memory data. Under program control, the system processor can read back and modify data stored in the VLT.

Although the backplane has no active electronic components, this hardware is considered a logical functional element of the 9460. Functionally, the backplane distributes control and data signals between the PCBs which mate via connectors. Operating voltage is also distributed by the backplane. Finally, the backplane provides strapping options which are part of the 9460

configuration control scheme.

<<<<<<<<<<<<<<<<<<<<Power Supply>>>>>>>>>>>>>>>>

(TBS)

Optional functional elements include:

- ¤ Processor expansion PCB
- ¤ High speed coordinate transformation (HSCT) PCB
- ¤ Pixel formatter PCB

The optional processor expansion PCB can add high speed mathematic logic, an IEEE-488 interface (not supported at this time), additional PROM, and additional RAM to the system processor PCB. High speed mathematic operations include fixed and floating point arithmetic and trigonometric functions. When configured, the processor expansion PCB works in conjunction with the system processor PCB during coordinate transformation processing. This PCB also has two RS 232 serial ports.

The HSCT PCB acts as an internal 9460 peripheral. When this PCB is installed the system processor PCB will route coordinate transformation or matrix operations to the HSCT PCB. In this way, the system processor PCB and MCP2 can continue to operate during coordinate transformation processing. Transformations include rotate, translate, and scale.

A pixel formatter PCB allows users to store pictures more compactly. (More)

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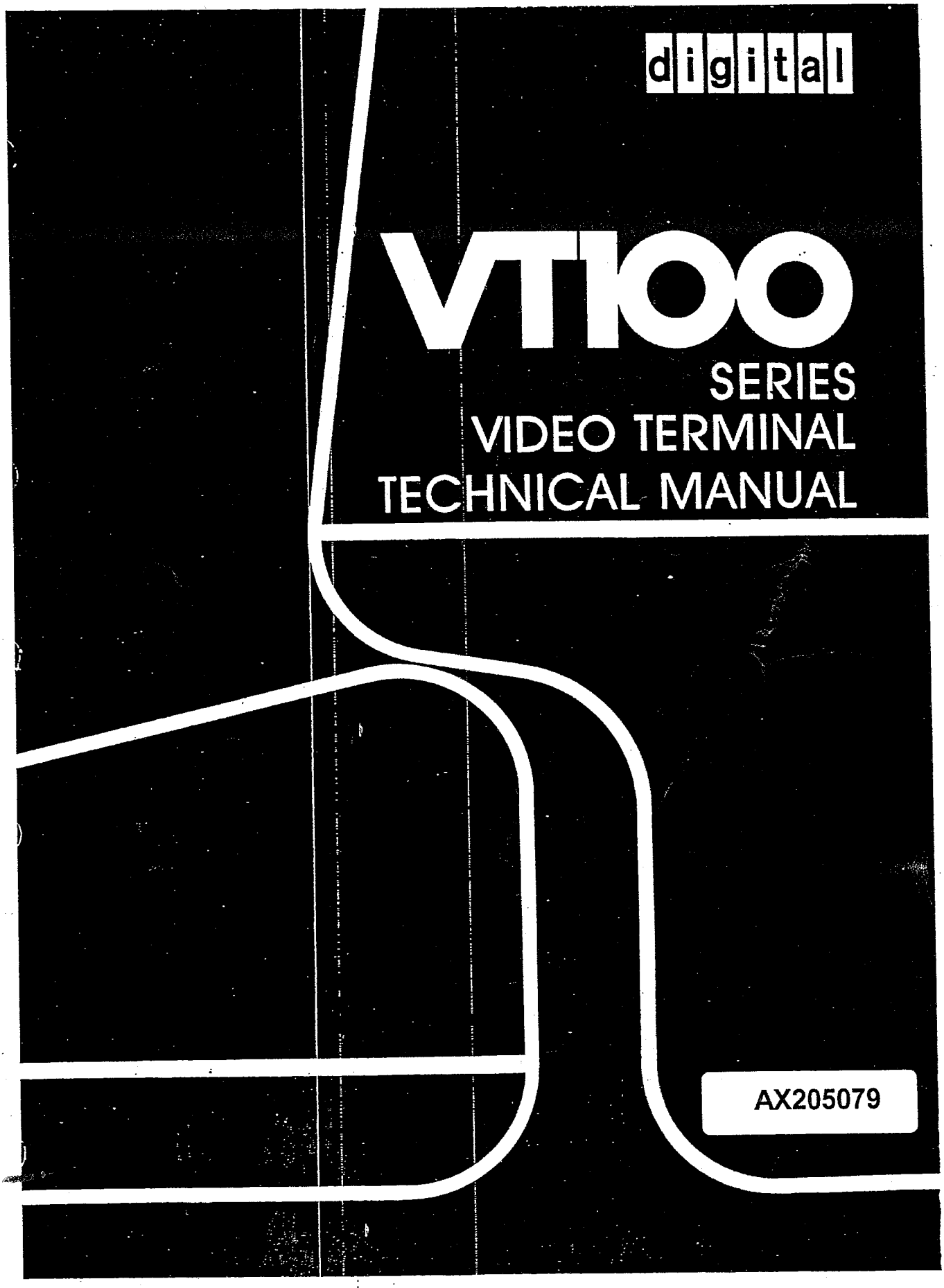
digital
VT100
SERIES
VIDEO TERMINAL
TECHNICAL MANUAL
AX205079

EK-VT100-TM-003

VT100 SERIES VIDEO TERMINAL TECHNICAL MANUAL

Prepared by Educational Services
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CHAPTER 1
INTRODUCTION AND SPECIFICATIONS

This is the technical manual for the VT100 series video terminals. It contains information a service technician or engineer needs to operate, test, and repair the VT100 series to a component level.

Chapter 1	Contains VT100 specifications and documentation ordering information.
Chapter 2	Contains basic operator information, including use of the keyboard, use of SET-UP modes for setting terminal characteristics, and simple trouble checking.
Chapter 3	Contains installation procedures and interface information.
Chapter 4	Contains a technical description of the basic VT100 video terminal. This chapter assumes that the reader has the Field Engineering Print Set, MP00633.
Chapter 5	Contains servicing information for the VT100 series video terminals.
Chapter 6	Contains SET-UP information for the various VT100 series options, installation information, a technical description, and service information for the Advanced Video option, Current Loop option, VT105 Graphics Processor, VT1XX-AC Printer option, and VT125 Graphics Processor.
Chapter 7	Contains a technical description and interfacing information for the standard terminal port (STP).
Chapter 8	Contains interfacing information for the graphics connector.
Appendix A	Contains programming information for the VT100 series, including interface timing considerations and descriptions of control functions the VT100 responds to, both in ANSI mode and in DEC VT52-compatible mode. Also contains copy of VT125 Programming Reference Card, EK-VT125-RC-001.
Appendix B	Contains a recommended spares list (RSL).
Appendix C	Contains a glossary of terms and abbreviations used in this manual.
Appendix D	Contains a description of the ANSI code extension techniques.

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VT100 SPECIFICATIONS

DIMENSIONS

Monitor	
Height	36.83 cm (14.5 inch)
Width	45.72 cm (18 inch)
Depth	36.20 cm (14.25 inch)
Keyboard	
Height	8.89 cm (3.5 inch)
Width	45.72 cm (18 inch)
Depth	20.32 cm (8 inch)
Minimum table depth	51.4 cm (20.25 inch)
Weight	
Monitor	13.6 kg (30 lb)
Keyboard	2.0 kg (4.5 lb)
Shipping weight	18.6 kg (41 lb)

ENVIRONMENTAL

Operating	
Temperature	10° to 40° C (50° to 104° F)
Relative humidity	10% to 90%
Maximum wet bulb	28° C (82° F)
Minimum dew point	2° C (36° F)
Altitude	2.4 km (8,000 ft)
Nonoperating	
Temperature	−40° to 66° C (−40° to 151° F)
Relative humidity	0 to 95%
Altitude	9.1 km (30,000 ft)

Power

Line voltage	90–128 V rms single phase, 2 wire 180–256 V rms single phase, 2 wire (switch-selectable)
Line frequency	47–63 Hz
Current	3.0 A rms maximum at 115 V rms 1.5 A rms maximum at 230 V rms
Input power	250 VA apparent 150 W max.
Current limiting	3 A normal blow fuse
Power cord	Detachable, 3 prong, 1.9 m (6 ft)

Display	
CRT	30 cm (12 inch) diagonal measure, P4 phosphor
Format	24 lines × 80 characters or 14 lines × 132 characters (selectable)
Character	7 × 9 dot matrix with descenders
Character size	
80 column mode	3.35 mm × 2.0 mm (0.132 inch × 0.078 inch)
132 column mode	3.35 mm × 1.3 mm (0.132 inch × 0.051 inch)
Active display size	203 mm × 127 mm (8 inch × 5 inch)
Character set	96-character displayable ASCII subset (upper- and lowercase, numeric, and punctuation)
Cursor type	Keyboard-selectable, blinking block character or blinking underline
Keyboard	
General	83-key detachable unit with 1.9 m (6 ft) coiled cord attached
Key layout	65-key arrangement and sculpturing similar to standard typewriter, with 18-key numeric keypad.
Numeric keypad	18-key with period, comma, minus, enter, and four general purpose function keys.
Visual indicators	7 LEDs; 3 dedicated to ON LINE, LOCAL, and KBD LOCKED; 4 are user-programmable.
Audible signals	
Keyclick	Sound simulates typewriter.
Bell	1) sounds upon receipt of BEL code; 2) sounds 8 characters from right margin (keyboard-selectable).
Multiple bell	Sounds upon detection of error in SET-UP save or recall operation.
Communication	
Type	EIA
Speeds	Full duplex: 50, 75, 110 (two stop bits), 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, 19,200
Code	ASCII
Character format	Asynchronous
Character size	7 or 8 bits; keyboard-selectable. (Note: if 8-bit character is selected, 8th bit is always space.)
Parity	Even, odd, or none (keyboard-selectable)
Synchronization	Keyboard-selectable via automatic generation of XON and XOFF control codes.

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ORDERING DOCUMENTATION

You can purchase the following VT100 series video terminal documents from DIGITAL's Accessories and Supplies Group.

Title	Part Number
VT100 User Guide	EK-VT100-UG
VT100 Series Pocket Service Guide	EK-VT100-J1
VT100 Illustrated Parts Breakdown (IPB)	EK-VT100-IP
VT100 Print Set (contains VT1XX-AC)	MP-00633
VT105 Technical Manual	EK-VT105-TM
VT105 Illustrated Parts Breakdown (IPB)	EK-VT105-IP
VT105 Print Set	MP-00642
VT125 User Guide	EK-VT125-UG
VT125 Print Set	MP-01053
VT1XX-CB, -CL Print Set	MP-01052
VT125 Illustrated Parts Breakdown (IPB)	EK-VT125-IP
VT132 User Guide	EK-VT132-UG
VT132 Print Set (contains VT1XX-AC)	MP-00748
VT132 Illustrated Parts Breakdown (IPB)	EK-VT125-IP
VT1XX-AC User Guide	EK-VT1AC-UG
VT1XX-AC Print Set	MP-00901

You can order accessories and supplies (including documentation) by mail or phone.

Continental USA

Call 800-258-1710 or mail order to:
Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

New Hampshire

Call 602-884-6660 or mail order to:
Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

Alaska or Hawaii

Call 408-734-4915 or mail order to:
Digital Equipment Corporation
632 Caribbean Drive
Sunnyvale, CA 94086

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Canada

Call 800-267-6146 or mail order to:
Digital Equipment Corporation
P.O. Box 13000
Kanata, Ontario Canada K2K 2A6
Att: A&SG Business Manager
Telex: 610-562-8732

Related Documentation

Intel 8080 Microcomputer Systems User's Manual
From: Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

EIA Specifications RS-232-C and RS-170
From: Electronic Industry Association
EIA Engineering Department
2001 Eye Street, N.W.
Washington, DC 20006

ANSI Standards X3.41-1974, X3.64-1977, 3.4-1977
From: Sales Department
American National Standards Institute
1430 Broadway
New York, NY 10018

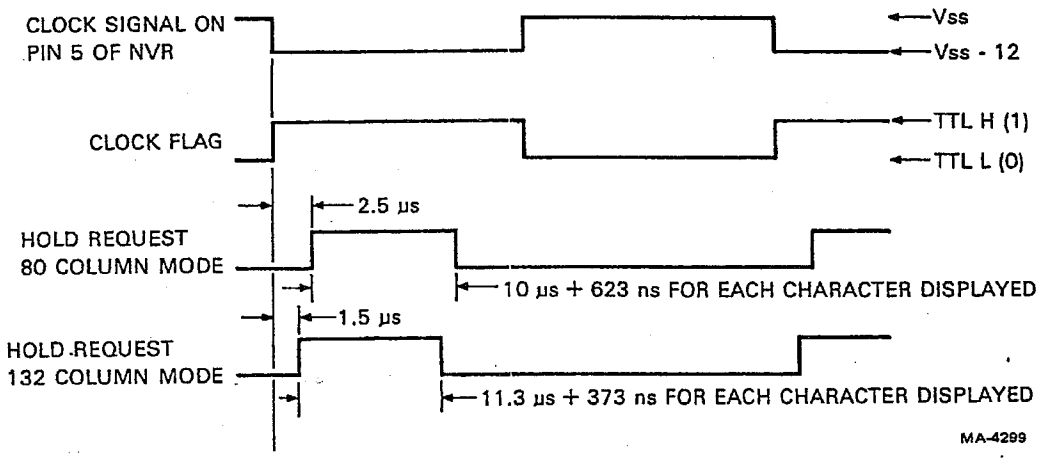

Figure 4-5-2 NVR Signals

All data and command changes to the ER1400 occur immediately following the falling edge of the clock flag (the rising edge of the signal on pin 5 of the ER1400); the data is strobed into the NVR on the opposite edge. The two one-of-ten codes for address have a single zero and nine ones (at D0 of the 8080 bus).

When the "shift data out" mode is entered as per the timing diagrams in Figure 4-5-3, the first data bit may appear when the mode is entered but will become stable 25 µs later; subsequent data bits will be shifted out on the falling edge of the clock flag (rising edge of the signal on pin 5 of the chip) and will become valid 25 µs later. This means that, following a change to "shift data out" mode or a falling edge of clock flag during this mode, a delay of 25 µs must occur before reading of the NVR data flag is attempted. The first bit shifted in when writing is the first bit shifted out when reading.

When using the ER1400, it is necessary to operate with interrupts off.

4.6 VIDEO PROCESSOR

The video processor is the heart of the VT100 display. It is composed of the devices shown on the right side of the terminal controller block diagram (Figure 4-6-1). This section discusses the general mechanism that converts data into a visible display, followed by a discussion of the two central devices (the timing and control chips) followed by a general discussion of all the other blocks on the video processor side of the block diagram. The interactions between the data paths on the left of the diagram and the processor on the right are covered in Section 4.7, Microprocessor – Video Processor Interface.

4.6.1 Introduction

The video processor converts data into an electrical signal that a CRT monitor can turn into visible letters, numbers, and symbols. The video processor works with the characteristics of the CRT monitor to do this. A brief description of these characteristics precedes an introduction to the video processor's operation.

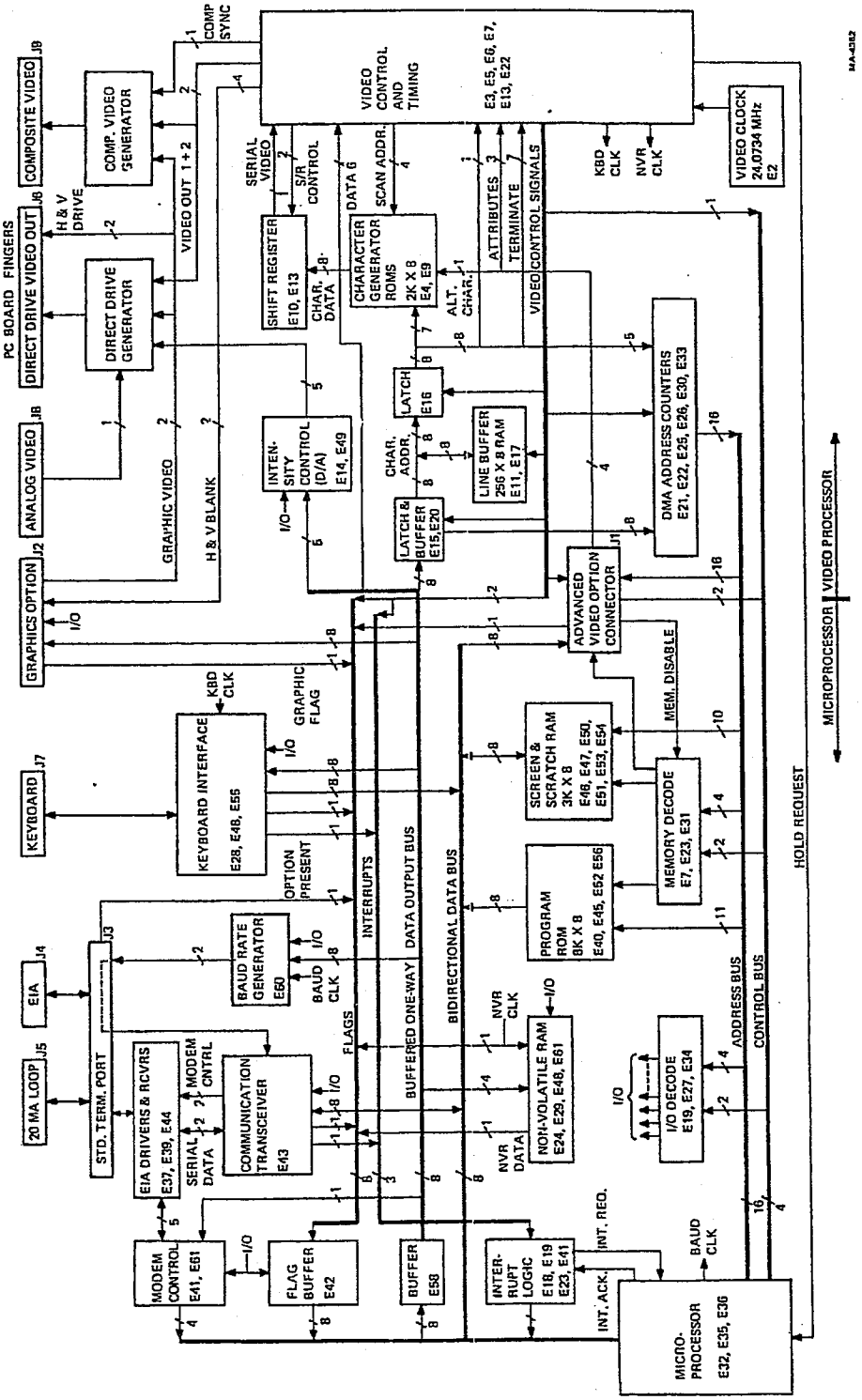

Figure 4-6-1 Video Processor Block Diagram

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4.6.1.1 The Raster – The raster is that area on the CRT screen that is scanned (passed over) by an electron beam moving in a regular pattern. Deflection coils cause the beam to quickly scan a series of horizontal lines while moving relatively slowly down the screen. This scanning repeats quickly and constantly, and persistence of vision makes the entire screen look continuously scanned. The beam may be on or off, lighting the fluorescent phosphor on the face of the CRT or leaving it dark, but the beam's continuous motion traces and defines the raster.

4.6.1.2 Character Formation – As the beam moves in its horizontal scans, it can be turned on and off very fast. This means that a spot of light (called a dot) can be produced anywhere along each horizontal scan line. Each scan contains the same number of potential dots. If only one dot is lit in a scan but dots in the same position on several successive scans are also lit, the screen appears to have a vertical line on it. This ability to line up dots on different scans is the key operating feature of the video processor.

Limiting our discussion to 80 column lines for this description, each character that can be displayed on the VT100 is made up of a matrix of dots, ten wide and ten high (Figure 4-6-2). There are 800 dots in a scan and the raster is made of 240 scans. So there are 80 groups of ten dots in each scan horizontally, and 24 groups of 10 scans vertically. Each 10 dot × 10 scan group is a character cell, where a character can be displayed, and there are 80 × 24 character cells on the screen. As the electron beam scans the raster, the video processor turns the beam on and off, assembling the characters scan by scan.

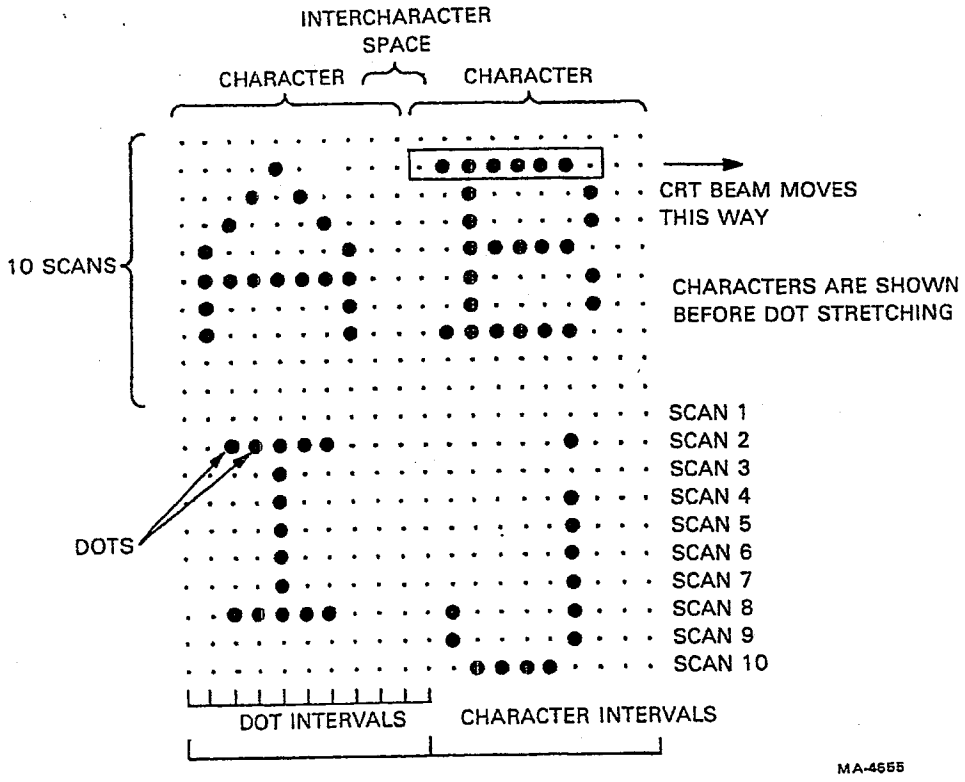

Figure 4-6-2 Dots, Scans, and Characters

4.6.1.3 Video Processor Data – When we say the characters are assembled scan by scan, we mean that only one scan of information about a character is displayed and then the same scan for the next character is displayed. This continues to the end of a line of characters. Then the next scan of the first character is displayed, followed by the same scan of the next character, and so on. Therefore, each character must enter the video processor ten times, once for each scan, and remain only until the next character in the line is displayed.

Each character in a line is stored in one of a group of adjoining locations in the screen RAM. (See Figure 4-6-3 for the video processor functional diagram.) The process of moving a line of character data from the screen RAM to the video processor takes the same amount of time as a scan. During data movement, the microprocessor cannot use the RAM. So, to give the microprocessor as much working time with the RAM as possible, the video processor accepts the line of character data for display during the first scan and stores it in its line buffer at the same time for use during the other nine scans. Movement of data from the screen RAM to the line buffer by the video processor is called direct memory access (DMA). During the DMA, the video processor provides addresses to the screen RAM with the address counters. The data is stored in the line buffer which gets its addresses from the line buffer address (LBA) outputs from the DC011 timing chip. Both kinds of addresses change values when they receive a clock (called character clock) that occurs after each 10 dots. This clock makes the character data in the video processor change at the right times to provide proper alignment of the display.

The character latches hold the data coming from the screen RAM or line buffer and ensure that the data remains stable for long enough periods to be written into the line buffer or the video shift register. The buffer between the latches is tristatable and, during non-DMA time, prevents the normal data flow on the microprocessor data bus from interfering with the video processor's reading of data from the line buffer.

4.6.1.4 Video Processor Character Generation – Data, coming either from the screen RAM for scan 1 or the line buffer for scans 2 through 10, becomes part of an address to a character generator ROM. (See Figure 4-6-4, Character Generator Example.) The rest of the address comes from a scan counter in the DC012 control chip. The scan counter addresses the ROM according to which of the ten scans is to be displayed. The 4-bit scan counter skips over the other 6 possible addresses to the ROM, so the ROM contains data in only 10 out of 16 locations. The output of the ROM is eight bits that represent the pattern of sequential dots to be displayed for that character on that scan. The eight bits enter the video shift register, a serializer that converts the eight parallel bits into a one-bit-wide stream. An extra flip-flop stores the last bit so it can be output to the stream two or three extra times (depending on line length) to fill the intercharacter space. The stream enters the DC012 control chip, where the final adjustments for video display are made, and then the video signal goes to the CRT monitor.

4.6.1.5 Attributes – Three attributes apply to the VT100 display: character, line, and screen. Character attributes provide a special appearance to characters as they appear on the CRT screen. In the basic VT100 (without an advanced video option) only one bit of memory (called the base-attribute bit) is available to each character on the screen. The original character data from the screen RAM is eight bits wide but only seven bits define the character itself. The eighth bit defines the base attribute. The attribute bit bypasses the character generator ROM and video shift register and enters the DC012. There it controls the presence or absence of the attribute as that character is displayed. The base attribute is displayed as either reverse video or underline, depending on the selection of the cursor at SET-UP, and is invoked by the base attribute bit. Reverse video appears as all 10 scans of a character cell reversed (black changes to white and vice versa). Thus, if two vertically adjacent characters are in reverse video, no black space appears between them. Underline forces the ninth scan on (off with reverse video screen attribute.) Once a character attribute or combination of attributes is set, all displayable characters sent to the terminal have that attribute regardless of where they are placed on the screen. This continues until the attribute selection is changed.

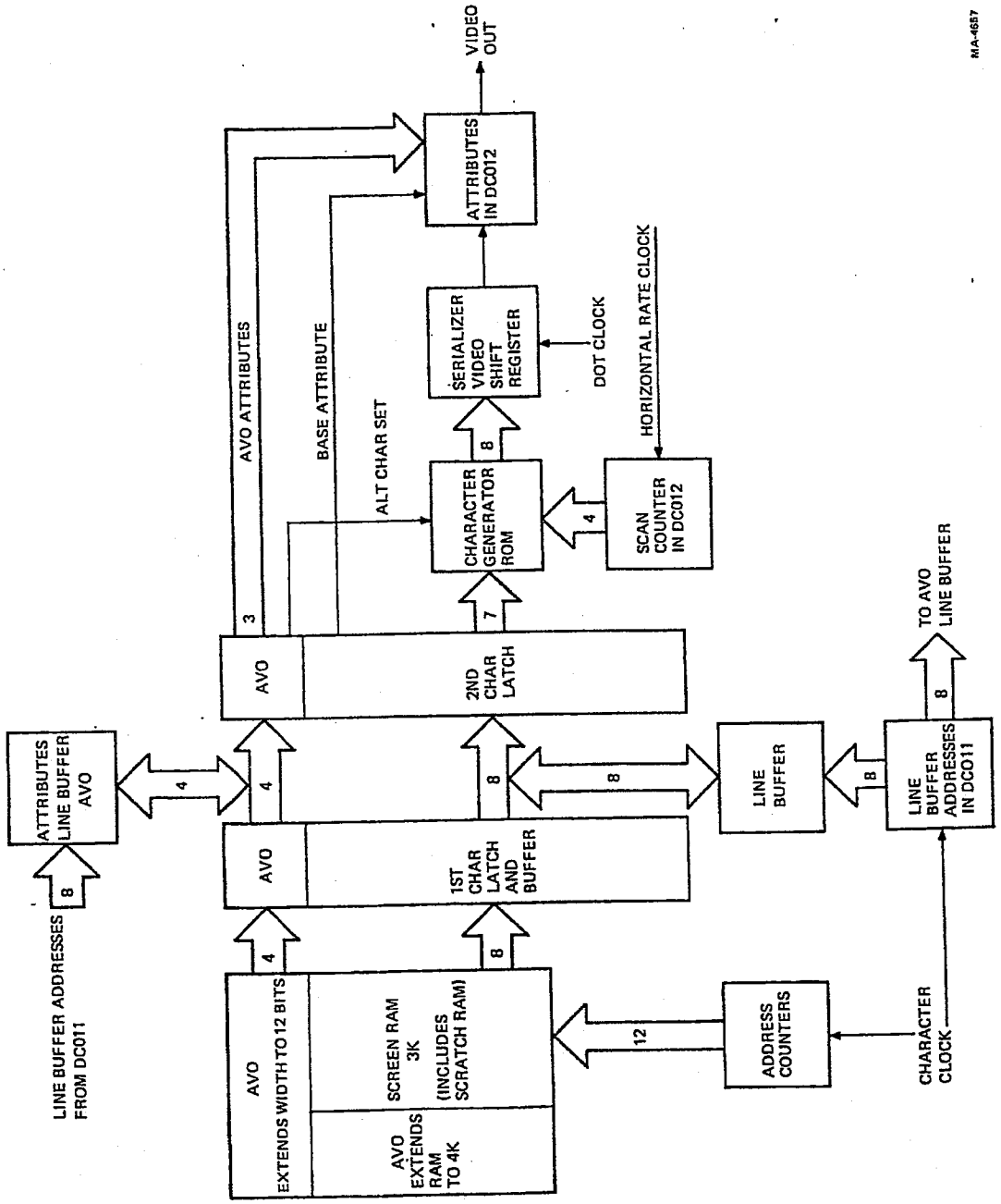

Figure 4-6-3 Video Processor Functional Diagram

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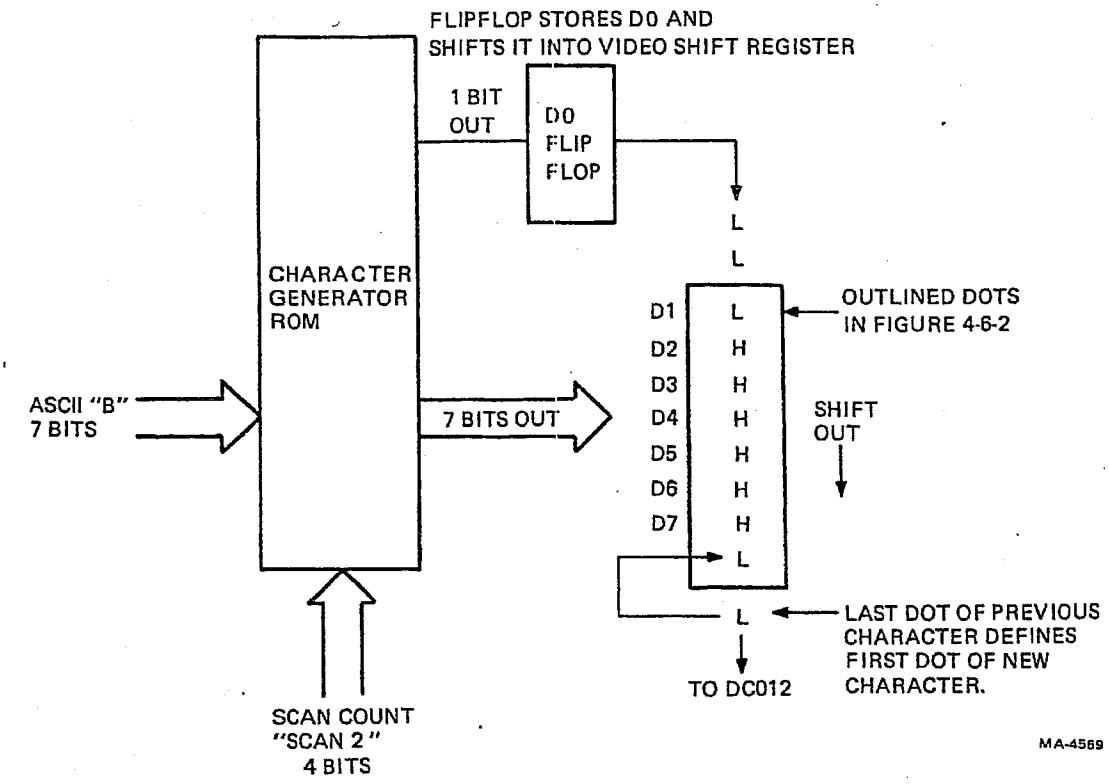

Figure 4-6-4 Character Generator Example

Line attributes are double height, double width, and scroll. The VT100 displays single-width, double-width or double-height, double-width characters on a line by line basis. All characters on one line appear in the same mode. Double-width lines are generated by displaying each dot of a character twice in the horizontal direction. Double-height, double-width lines are generated by displaying each dot of a character four times (twice horizontally and twice vertically). The top and bottom halves of a double-height, double-width line must be entered as two separate lines of characters. The scroll attribute indicates that a line is part of the scrolling region.

Screen attributes affect the entire screen's characteristics at once. They include the base attribute selection (reverse or underline as mentioned under character attributes), reverse video over the entire screen, 80 or 132 character line length, 50 or 60 Hz refresh rate (chosen according to the local power supply), interlaced or noninterlaced operation, and jump or smooth scrolling of data over the screen.

4.6.1.6 Advanced Video Option (AVO) – The AVO extends the length of the screen RAM so more characters can be displayed in 132 column mode. In addition, it allows each character to have four more attributes, for a total of five. Three of the AVO attribute bits enter the DC012 to control displayable features of each character. The fourth AVO attribute bit controls the selection of an extra character set by switching in an optional alternate character generator ROM that can provide non-ASCII characters or other special displays.

To provide the extra attribute bits, the AVO widens the entire screen RAM by 4 bits to make each character location 12 bits wide. It also contains a 4-bit wide extension of the character latches and a 4-bit wide attribute line buffer, addressed by the same LBA signals as the regular line buffer. This extension treats the attribute data with the same timing as the character part of the circuit, and matches each character with its attributes.

With the AVO present, reverse video, underline, bold, and blinking are all available singly or in combination. Reverse and underline appear as described above with the addition that if both reverse and underline are asserted, the underscore is forced dark instead of light. Bold increases the intensity of the display. The blink rate is about half that of the cursor or about 0.5 Hz. Cursor selection is independent of character attributes when the AVO is installed.

4.6.2 Timing Chip Description

The DC011 is a custom designed bipolar integrated circuit that provides most of the timing signals required by the video processor. Internal counters divide the output of a 24.0734 MHz oscillator (located elsewhere on the terminal controller module) into the lower frequencies that define dot, character, scan, and frame timing. The counters are programmable through various input pins to control the number of characters per line, the frequency at which the screen is refreshed, and whether the display is interlaced or noninterlaced. These parameters can be controlled through SET-UP mode or by the host. In the following discussion, refer to the block diagram in Figure 4-6-5.

4.6.2.1 Input Decoder – The input decoder responds to commands on the D0 H and D1 H pins (connected to D4 and D5 of the 8080 bus respectively) whenever the VIDEO WR 1 L pin is low. The outputs of the decoder select 80/132 column, 60/50 hertz refresh, and interlaced/noninterlaced modes of operation. Table 4-6-1 shows that when D1 H is low the number of columns is programmed according to the state of D0 H, and when D1 H is high the refresh rate is programmed. Interlaced mode is always selected when the column mode is set, and noninterlaced mode is selected when the refresh rate is set. The interlace mode in use depends on whether "number of columns" or "refresh rate" was selected last.

Table 4-6-1 Video Mode Selection
(Write Address = C2H)

Inputs			
D5 Pin 21	D4 Pin 20	Configuration	
0	0	80 column mode	Sets interlaced mode
0	1	132 column mode	
1	0	60 hertz mode	Sets noninterlaced mode
1	1	50 hertz mode	

In addition to strobing data into the input decoder, VID WR 1 L also acts as a reset signal for the DC011. Whenever VID WR 1 L is low, the counters in the DC011 are held in a cleared state. Resetting the counters serves no purpose in the VT100 because the remainder of the VT100 synchronizes itself to the DC011, but a reset is useful for testing both individual chips and complete modules. Because writing into the DC011 would cause the counters to reset and disturb the display, this is never done unless the mode is being changed.

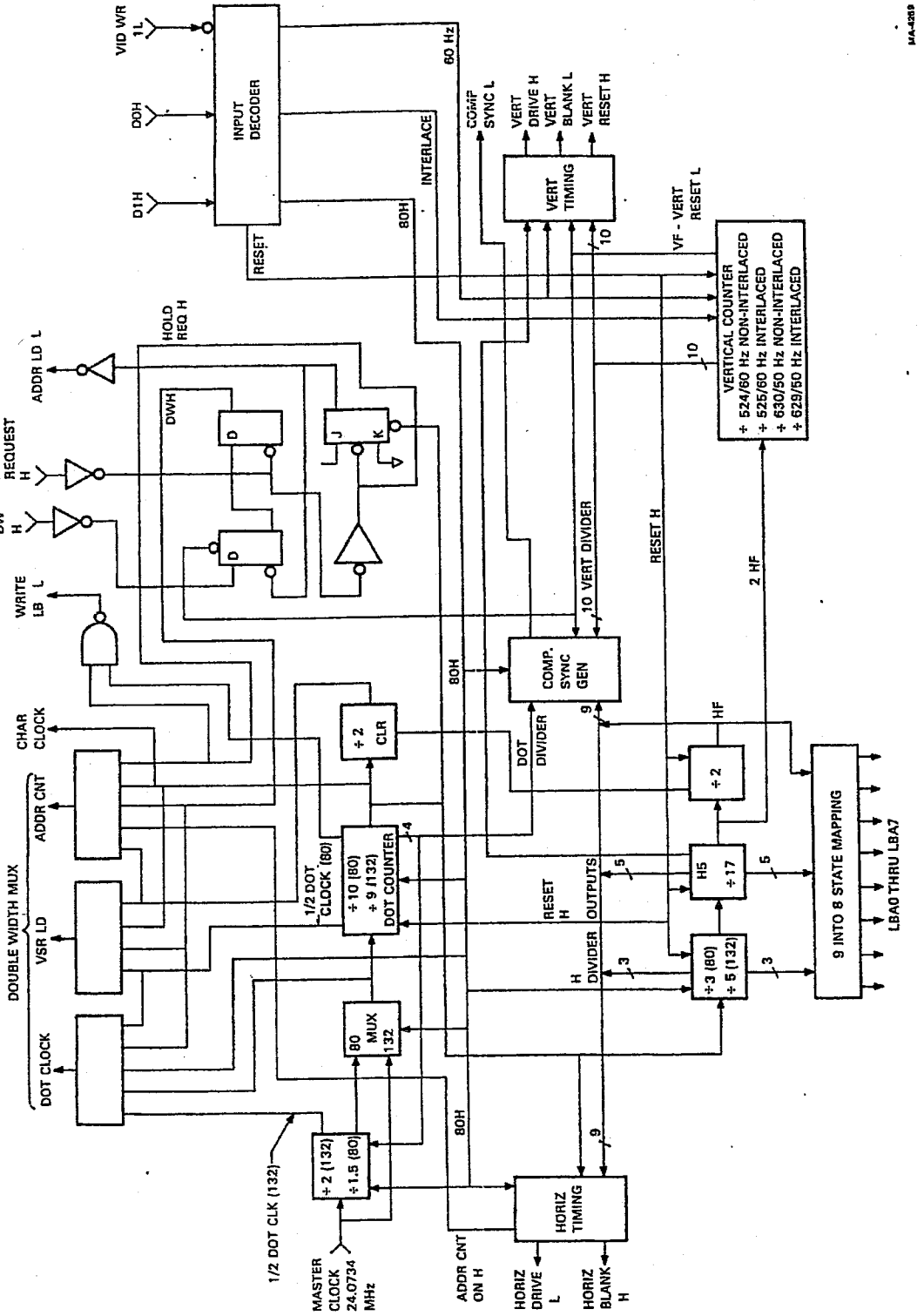

Figure 4-6-5 DC011 Block Diagram

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4.6.2.2 80/132 Column Selection – The column mode is changed by modifying the divisors of three of the counters in the DC011. The first of these counters divides the input clock (MASTER CLK) by 1.5 to produce the dot rate clock for 80 column mode. The DOT CLK output provides the signal that controls the shifting of dots out from the video shift register. A multiplexer determines what rate DOT CLK will have for the entire screen by selecting either the output of the divide-by-1.5 in 80 column mode, or by selecting the 24 MHz MASTER CLK directly in 132 column mode. The other two counters affected by 80/132 selection are the dot counter and the horizontal counter.

4.6.2.3 Dot Counter – The dot counter uses four flip-flops to divide the DOT CLK that was selected by the multiplexer by 10, in 80 column mode, or by 9, in 132 column mode. The output of the dot counter is the character rate clock, which is used to move character codes in the latches that are outside the DC011. Character clock is further divided by the horizontal counter. The timing of CHAR CLK is shown in Figures 4-6-6 and 4-6-7 for each of the two column modes. CHAR CLK is unaffected by double-width mode. The output of the next-to-last flip-flop is used for the write enable signal for the line buffer RAMs (WRITE LB L). WRITE LB L is also shown in Figures 4-6-6 and 4-6-7. This signal allows the data and address changes, caused by the rising edge of CHAR CLK, to become stable before writing is enabled and then disables writing before CHAR CLK rises again. WRITE LB L is gated directly with HOLD REQ H so that it is active only during DMAs. Intermediate signals from the four flip-flops are used by various other functions in the DC011 such as the double-width multiplexer and the composite sync generator.

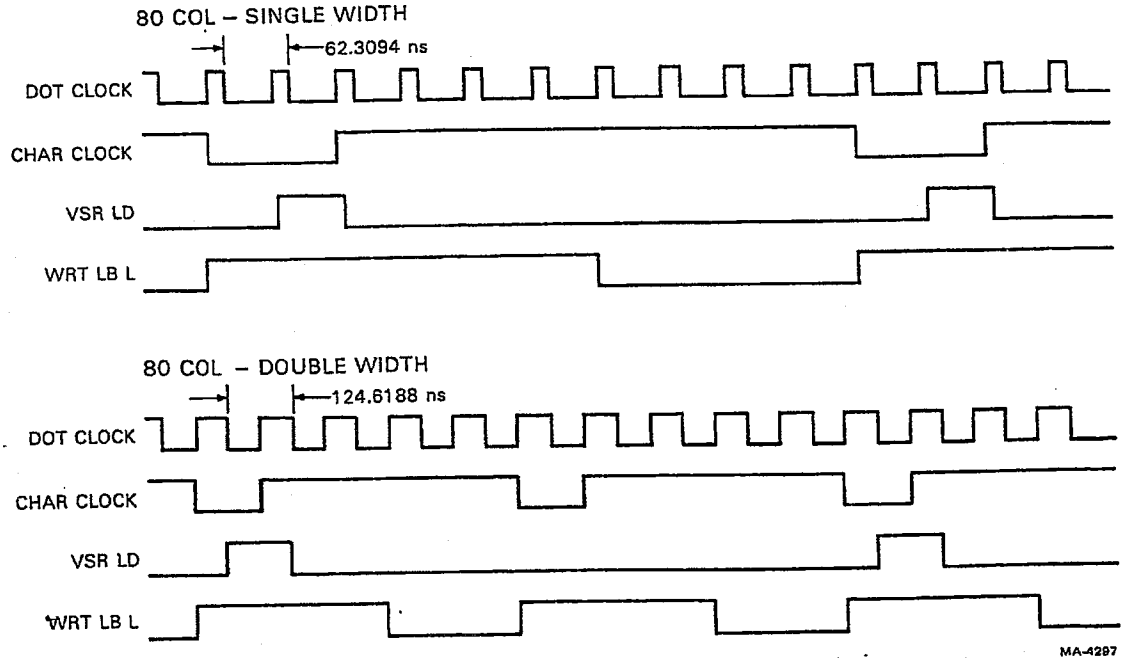


Figure 4-6-6 Video Latch Timing – 80 Column

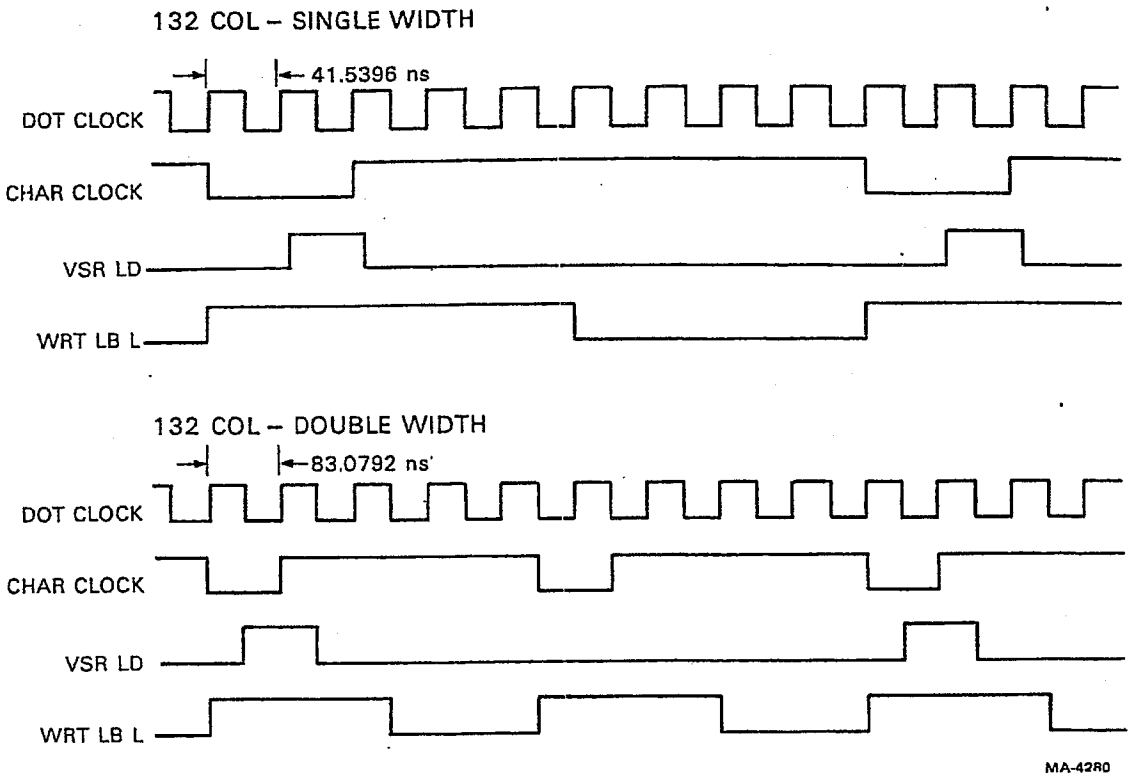


Figure 4-6-7 Video Latch Timing – 132 Column

4.6.2.4 Double-Width Multiplexer – The double-width multiplexer (MUX) produces the three signals whose timing must be changed when a line of characters is switched between single- and double-width modes. The frequency of DOT CLK must be divided in half on a double-width line so that the video shift register will shift half as often, making each dot (and therefore each character) twice as wide as it would be in single-width mode. In order for the video shift register to work properly with the half-rate DOT CLK in double-width mode, the load signal for the shift register (VSR LD H) must still come every 10 dots (80 column mode) or 9 dots (132 column mode). Therefore loads must occur at every other CHAR CLK. Similarly, incrementing the DMA address counters occurs on every other CHAR CLK to ensure that characters that are stored sequentially in the screen RAM are presented to the shift register at the correct time for each VSR LD H pulse. The different modes of DOT CLK and VSR LD H are shown in Figures 4-6-6 and 4-6-7.

In single-width mode, the double-width MUX directs the output of the 80/132 MUX to the DOT CLK pin, providing either a 16 MHz or 24 MHz output. To get the half-rate DOT CLK for 80 column mode, the double-width MUX selects the output of the first flip-flop in the dot counter, that acts as a divide-by-2 because the dot counter is dividing by 10 (10 is an even number). In 132 column mode the same selection cannot be made because the dot counter is dividing by 9. But the divide-by-1.5 is not needed in 132 column mode, so this divider is converted to a divide-by-2 and the double-width MUX selects its output when a double-width line is displayed in 132 column mode.

The load input of the video shift register used in the VT100 is a synchronous input. This means that when the load input is high, the rising edge of DOT CLK causes a parallel load to be performed instead of a shift. To get one load and many shifts for each character, VSR LD H can only last for that one cycle of DOT CLK that is adjacent to CHAR CLK. Furthermore, transitions of VSR LD H must satisfy SET-UP and hold times with respect to the rising edge of DOT CLK. In single-width modes, VSR LD H is one dot time wide, generated from the outputs of the dot counter, and its SET-UP and hold times are guaranteed by internal propagation delays. This relationship is shown in Figures 4-6-6 and 4-6-7 by a slight shift in the transitions of VSR LD H with respect to DOT CLK. In double-width mode, VSR LD H is created by selecting every other CHAR CLK (Figure 4-6-5 shows a flip-flop that divides CHAR CLK by two for this purpose) and then delaying this signal by one single-width dot time.

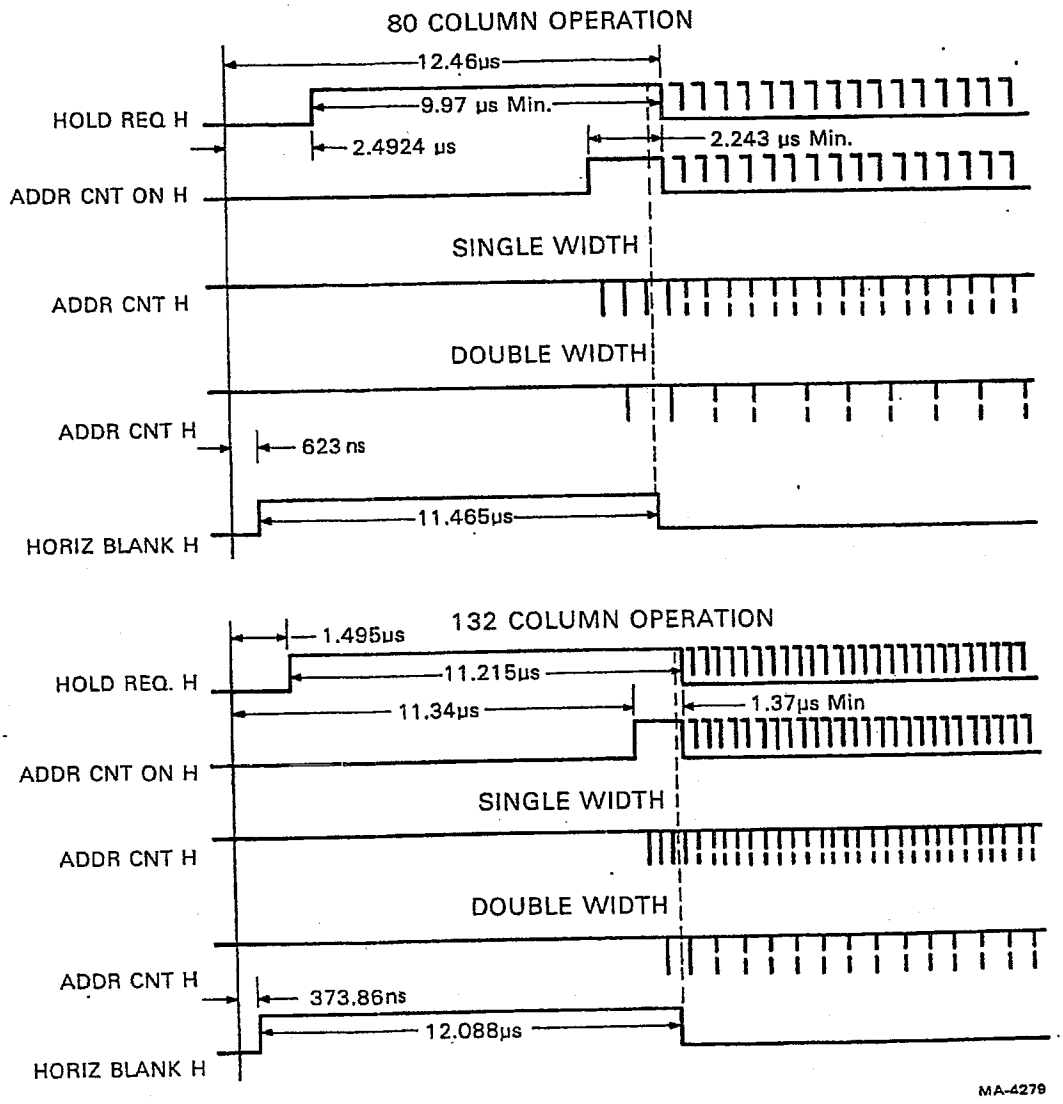


Figure 4-6-8 Address Count Timing

The signal that increments the DMA address counter (ADDR CNT) is shown in Figure 4-6-8. ADDR CNT has the same timing as CHAR CLK; the difference is that it does not run continuously. Figure 4-6-8 shows that ADDR CNT can only be generated if HOLD REQUEST H is high and that it is further controlled by a signal from the horizontal timing section (ADDR CNT ON H) that allows ADDR CNT to provide exactly three pulses (in single-width mode) before HORIZ BLANK H goes low. The three pulse delay primes the external character latches so that the dots for the first character on a line are being loaded into the video shift register at the same moment that HORIZ BLANK H enables the video at the beginning of a scan. The only change made to ADDR CNT for double-width operation is that every other pulse is deleted, beginning with the first pulse (Figure 4-6-8).

4.6.2.5 Horizontal Counter – The block diagram in Figure 4-6-5 shows the horizontal divider broken into three stages. The first divider is programmable according to the number of columns selected and is driven by CHAR CLK from the dot counter. For 80 column mode the divisor is three; for 132 column mode the divisor is five. The total division from MASTER CLK to the output of this first divider is 45, independent of mode (for 80 columns: $1.5 \times 10 \times 3 = 45$, for 132 columns: $1 \times 9 \times 5 = 45$). Therefore, the operation of all of the remaining dividers in the DC011, which are driven from the first horizontal counter, are also independent of the column mode. The second stage of the horizontal divider has a divisor of 17, which is chosen to give the required number of displayable columns plus about 28 percent more to allow time for the monitor to execute a horizontal retrace. The last stage is a simple divide-by-2 that provides the horizontal frequency. Designing the last stage to be a divide-by-2 guarantees that the signal at its input will have a frequency twice that of the horizontal frequency as required by the vertical dividers to create interlaced operation. The total division from CHAR CLK provided by the horizontal divider is 102 in 80 column mode and 170 in 132 column mode. In either mode the frequency at the output of the horizontal counter is 15.734 kHz.

4.6.2.6 Horizontal Drive and Horizontal Blank – Two timing signals are generated from the horizontal counter to control those system functions occurring at the scan rate. These signals begin at the end of a scan and last until the horizontal counter is incremented past a specific state that is decoded to turn the signals off. The monitor requires a pulse at the end of every scan to tell it when to initiate a retrace and begin the next scan; the duration of this pulse must be between approximately one-quarter and one-half of one scan. Figure 4-6-9 shows HORIZ DRIVE L as produced by the DC011; the slight difference in timing between 80 and 132 column modes is the result of design convenience and is not significant to the operation of the VT100. HORIZ BLANK H is designed to allow 83 characters during the forward scan in 80 column mode and 137 characters in 132 column mode. The extra characters are included for possible future use such as a field of indicators along the right margin of the screen or as extra symbols inserted to mark text. The rising edge of HORIZ BLANK H is synchronized to CHAR CLK to eliminate the accumulated delay of the horizontal counter. The falling edge of HORIZ BLANK H occurs between two CHAR CLKs (Figure 4-6-8) to meet some requirements of the DC012, but inside the DC012 HORIZ BLANK H is delayed to the following edge of CHAR CLK so that the beginning of each displayed scan will coincide with a character boundary. The actual video blanking occurs inside the DC012. Therefore there is no signal outside the DC012 that has the exact length of horizontal blank time.

4.6.2.7 Line Buffer Addressing – The line buffer memory stores one line of characters during a scan on which a DMA occurs and then recalls these characters on each successive scan until the next DMA. Because the line buffer is a random access memory, it has address inputs that must be provided with a sequence of addresses that change at each CHAR CLK such that each character is stored in a unique location. The horizontal counter can provide such addresses because it is incremented through a series of unique states that repeat in the same sequence on every scan. Because of the three stages that comprise the horizontal counter, there are nine flip-flops whose outputs must be converted into the eight line buffer address (LBAs) outputs. The conversion is possible because the 9 flip-flops represent a maximum of 170 states in 132 column mode (8 bits can represent 256 states). The DC011 contains gates that combine the output of the ninth flip-flop in the horizontal counter with the outputs of the other

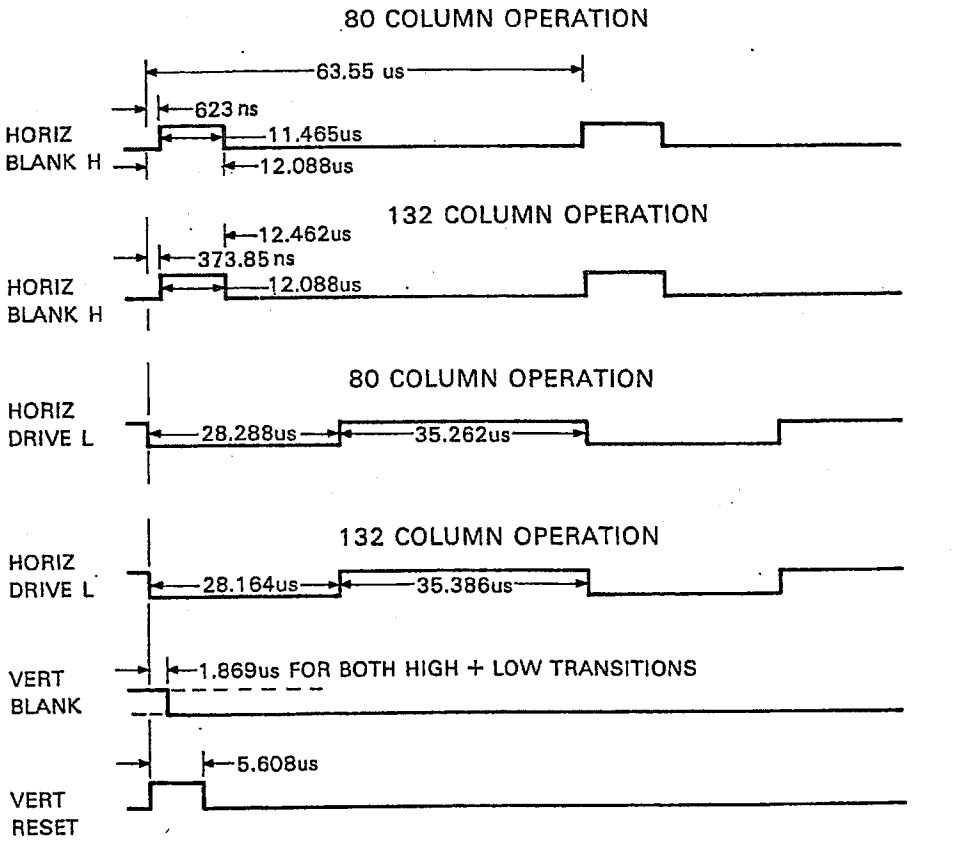


Figure 4-6-9 Horizontal Timing

eight to generate some addresses that are not otherwise represented by the eight. The resulting LBAs do not follow a normal binary counting sequence but the sequence of unique addresses repeats exactly on each scan. Figures 4-6-10 and 4-6-11 show the LBA sequence for one-half of a scan; the other half is identical except that LBA 7 is low.

Several of the LBAs are used as general purpose clocks in the VT100. LBA 3 and LBA 4 are used to generate timing for the keyboard. These signals satisfy the keyboard's requirement of two square-waves, one twice the frequency of the other, even though every 16th transition is delayed (the second stage of the horizontal counter divides by 17, not 16). LBA 7 is used by the nonvolatile RAM. The 31.468 kHz signal on LBA 6 could be used for power supply synchronization, although this is not done in the VT100.

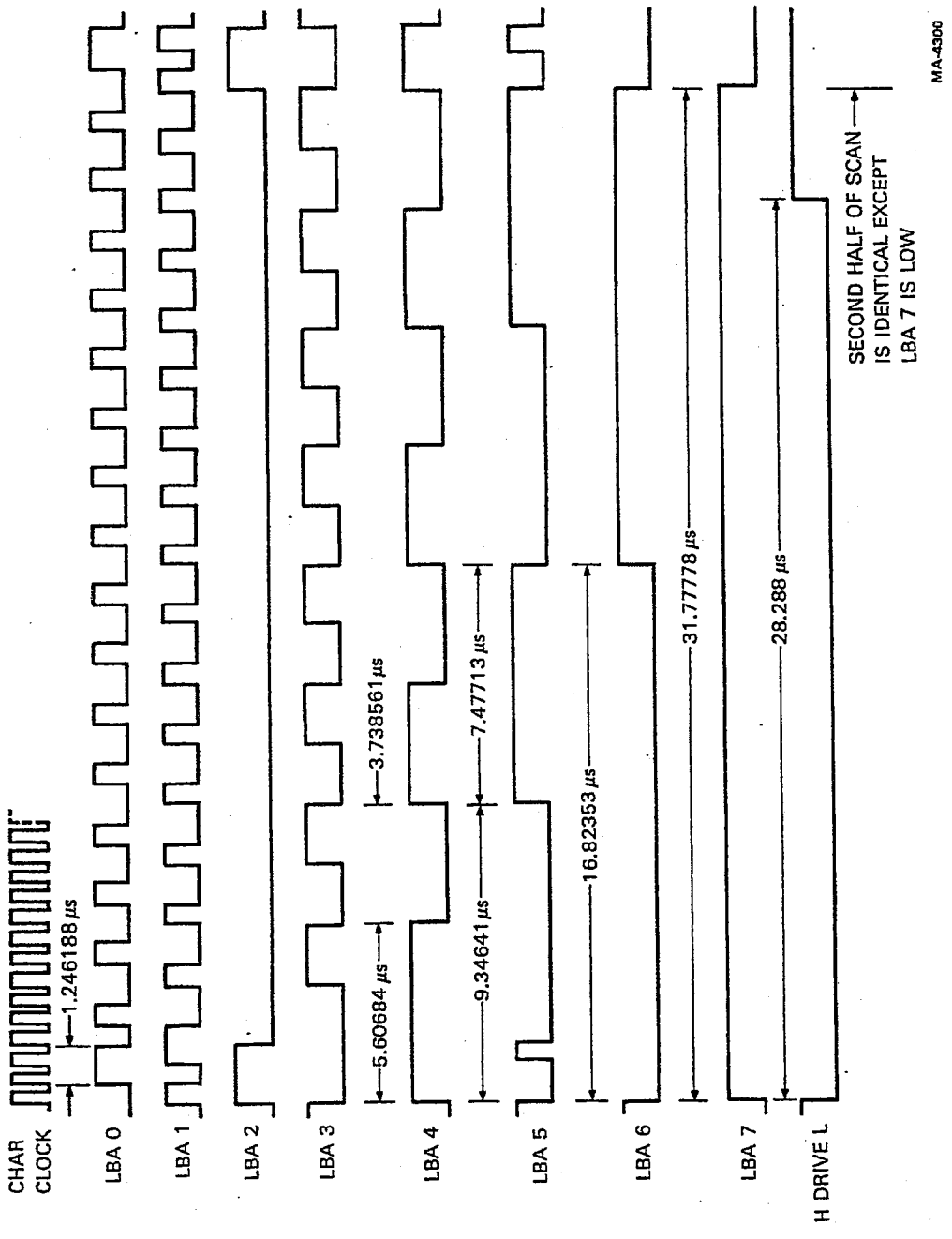


Figure 4-6-10 Line Buffer Address Outputs – 80 Column

AX205190

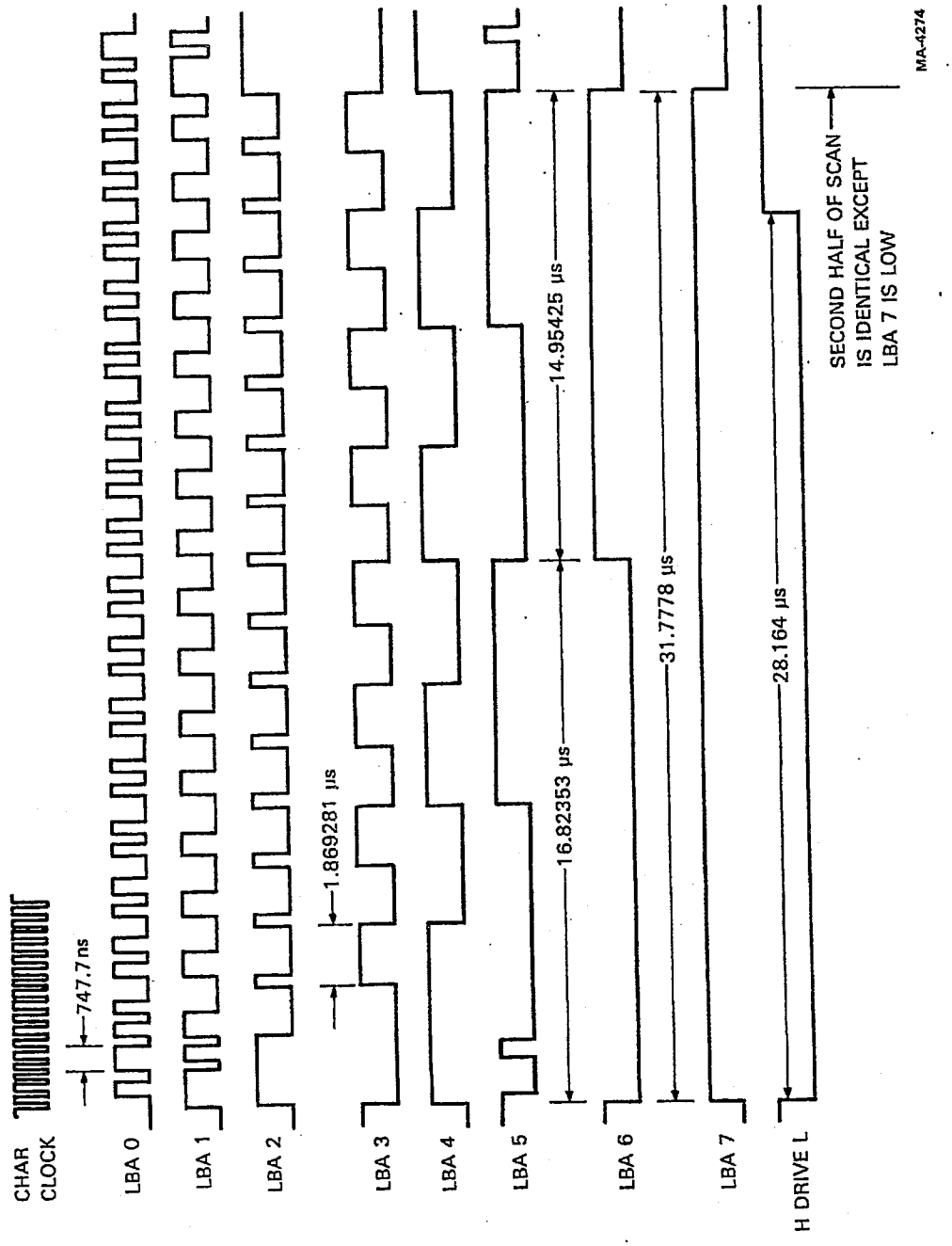


Figure 4-6-11 Line Buffer Address Outputs – 132 Column

4.6.2.8 Vertical Operation – To paint a complete picture on the screen, the monitor moves the electron beam slowly from the top of the screen to the bottom, while it is also moving the beam quickly from left to right to paint each scan. The vertical sweeps of the beam must be repeated continuously so that the picture is refreshed often enough to prevent the appearance of flicker. In television terminology, a single pass of the beam from the top of the screen to the bottom (and the data displayed during that time) are referred to as one field. A complete picture, which may contain one or more fields depending on the type of interlacing in use, is called one frame. When the VT100 is used in noninterlaced mode, each successive field is identical and therefore only one field is contained in each frame. During interlaced operation in the VT100, there are two types of fields that alternate with each other so that each frame consists of two fields. Even fields start at the top of the screen and display 240 scan lines before reaching the bottom. Odd fields place their first scan line between the first and second scans of the preceding even field and then place each additional scan between succeeding scans of the even field. Interlacing the even and odd fields gives a whole frame of 480 scans, instead of 240 scans, to provide increased vertical resolution. In noninterlaced operation, commands to the monitor to begin a new field are always coincident with commands to begin a new scan. This causes the beam to always be in the same vertical position when the first displayed scan is begun. But, in interlaced mode, odd fields begin with a command for a new frame that occurs halfway through a scan line. This causes the beam to have moved down the screen from where it would have been during an even field (by the distance that it moves in one-half of a scan) when the first displayed scan is begun. Even and odd fields are made to alternate by including an odd number of half-scans in every field. This is in contrast to noninterlaced operation, where each field contains only complete scans. The VT100 always displays the same video information on both even and odd fields. Interlaced mode is provided for future use by options that desire increased vertical resolution.

4.6.2.9 Vertical Counter – The 10-bit vertical counter, shown in Figure 4-6-5, determines the frequency at which the screen is refreshed by counting the number of horizontal scans to be included in each field. The vertical counter uses the 31.468 kHz output of the horizontal counter so that it can count the half-scans required for interlaced operation. Figure 4-6-5 lists the four available divisors that select the interlace mode and keep the refresh frequency as close to the local power line frequency as possible (to minimize interference with the screen from nearby equipment). The vertical frequencies produced by these divisors are approximately 1/20 Hz above or below the nominal power line frequency.

4.6.2.10 Vertical Outputs – Three outputs are derived from the flip-flops in the vertical counter to control the vertical refresh operations in the VT100. These signals are shown in Figures 4-6-12 and 4-6-13 for all four modes. VERT DRIVE H is issued at the bottom of the screen to initiate a vertical retrace followed by a new vertical scan. This operation is analogous to the effect of HORIZ DRIVE L on horizontal scans. The time between any two VERT DRIVE Hs is a constant, equal to an even number of half-scans in noninterlaced mode and equal to an odd number of half-scans in interlaced mode. VERT BLANK L always enables exactly 240 scans during any field and blanks any remaining scans. Furthermore, VERT BLANK L is always turned off exactly 20 scans after VERT RESET H in 60 Hz mode and 50 scans after VERT RESET H in 50 Hz mode. VERT BLANK L is always adjusted to display complete scans even during odd fields in interlaced mode. VERT RESET H initiates the DMA process at the start of every field. When VERT RESET H goes high, the DMA address counters are reset to point to address 2000H in the screen RAM, all line attributes are cleared, and the scroll counter in the DC012 is preset to the value stored in the scroll latch. (See the DC012 description for more explanation.) During noninterlaced operation and on even fields, VERT RESET H occurs at the same time as VERT DRIVE H; but, on odd fields VERT RESET H is delayed one-half of a scan to match the start of a horizontal scan. The relationship of VERT RESET H and transitions of VERT BLANK L to HORIZ BLANK H and HORIZ DRIVE L is depicted in Figure 4-6-9. Notice that VERT BLANK L always turns on or off when the video is already blanked by HORIZ BLANK H.

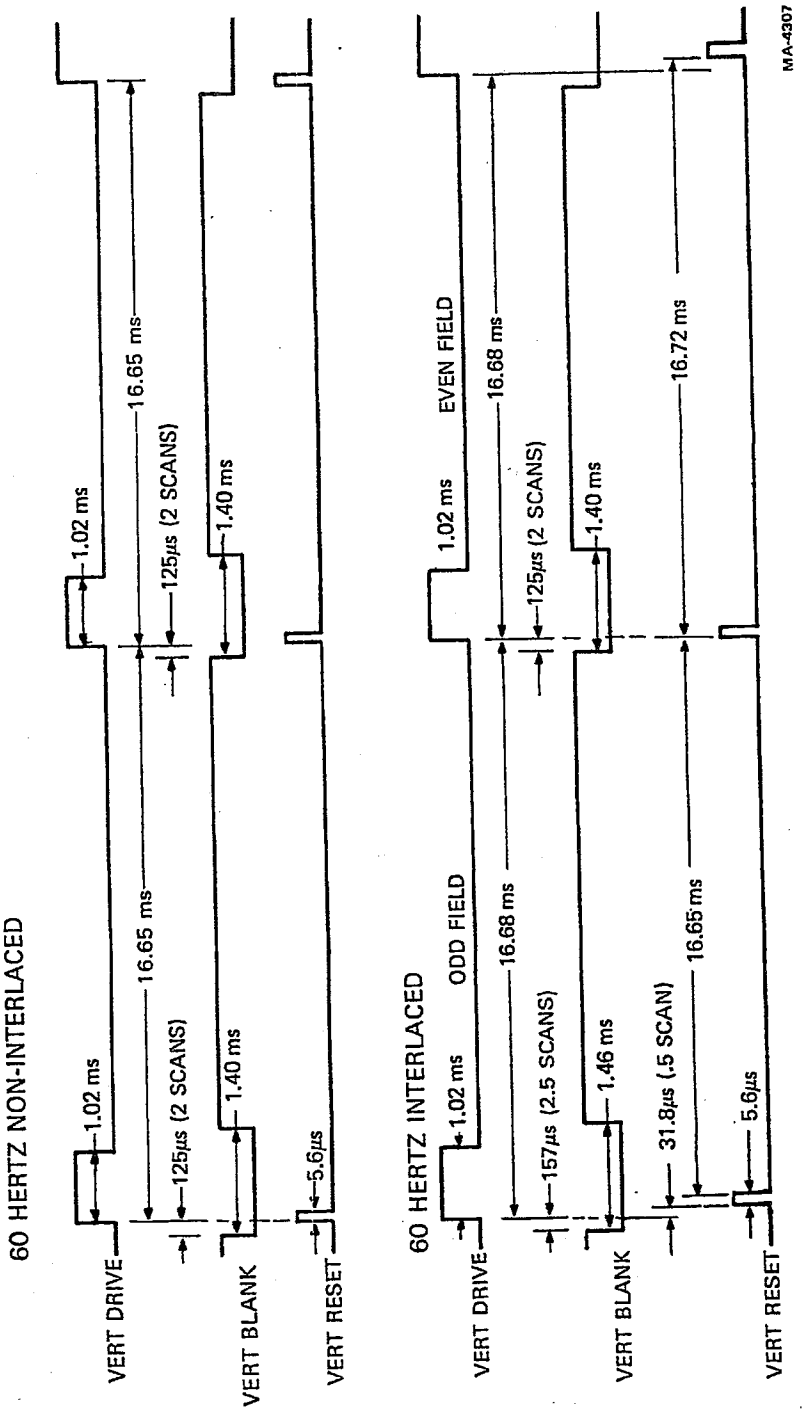


Figure 4-6-12 Vertical Signals – 60 Hz

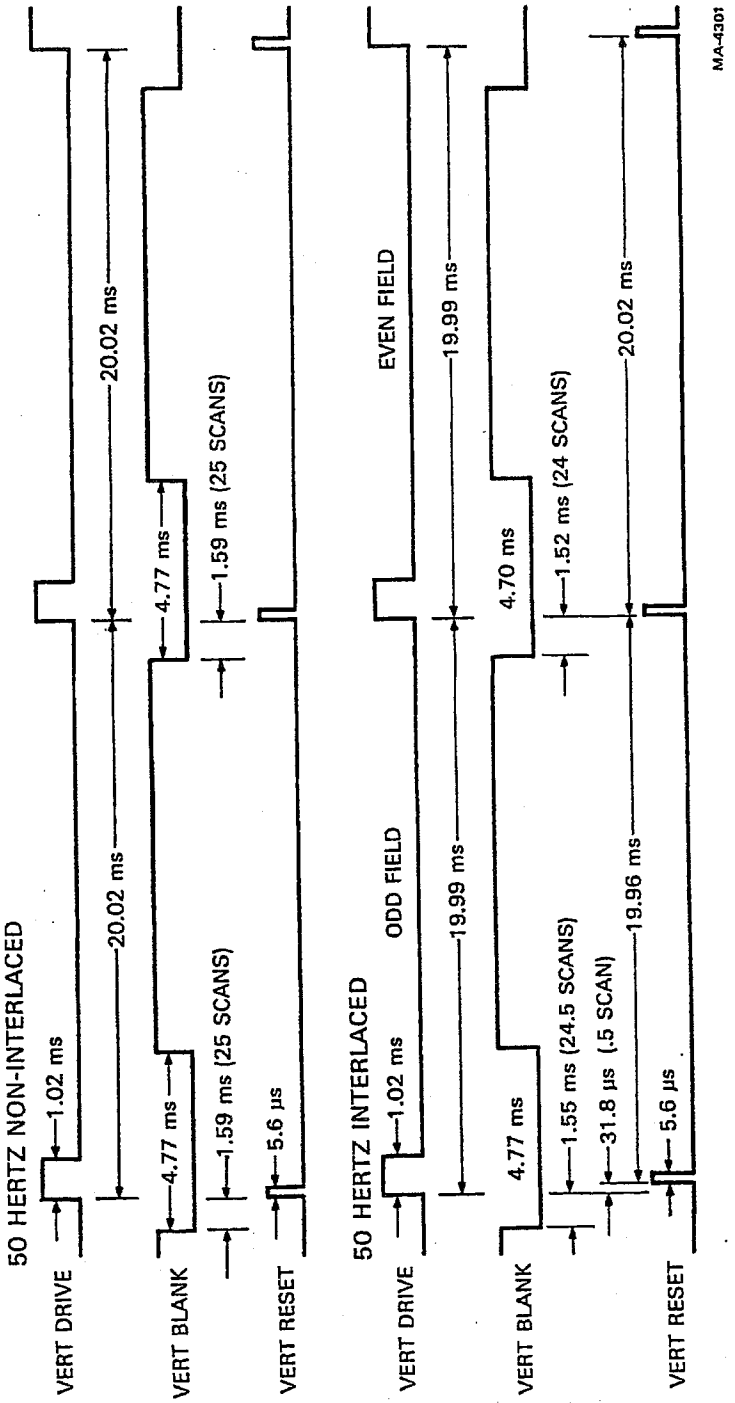


Figure 4-6-13 Vertical Signals – 50 Hz

AX205194

4.6.2.11 Composite Sync – The COMP SYNC L signal supplied by the DC011 is combined with video information by the terminal controller board to produce the composite video signal that appears on J9 at the back of the VT100. An external monitor can use the composite video signal to reproduce the image displayed on the VT100 screen. This is accomplished by using the video information to control beam intensity and the composite sync waveform to synchronize the raster to the video information. The composite sync generator in the DC011 uses outputs from the dot, horizontal, and vertical counters to generate the complex timing of COMP SYNC L. COMP SYNC L consists of one of the vertical intervals depicted in Figure 4-6-14 followed by 240 horizontal sync pulses, another vertical interval, etc. The vertical synchronizing interval consists of a transition from horizontal sync pulses to six equalizing pulses, six vertical sync pulses, six more equalizing pulses, and then a return to horizontal sync pulses. Two vertical intervals are shown in Figure 4-6-14. The vertical interval that begins an odd field is similar to that which begins an even field except that the equalization and vertical sync pulses are shifted by one-half scan with respect to the horizontal sync pulses. In noninterlaced mode all fields are even fields; but, in interlaced mode every other field is an odd field. Figure 4-6-14 also shows the relationship of COMP SYNC L to both the horizontal blank time (HORIZ BLANK H modified by the DC012) and VERT BLANK L. COMP SYNC L meets the requirements of EIA RS-170 and the NTSC standards for sync pulse generators.

4.6.2.12 Hold Request, Address Load, and Double-Width – The logic associated with HOLD REQ H, ADDR LD L, and DW H is shown in Figure 4-6-5. The falling edge of HOLD REQ H sets ADDR LD L to the low state; ADDR LD L is subsequently cleared by the falling edge of CHAR CLK, thus creating a short low pulse on ADDR LD L at the end of each DMA. ADDR LD L stores, in their respective registers, all line attributes and the memory address of the next line to be accessed by a DMA. The rising edge of HOLD REQ H causes the value of DW H that was stored in the holding flip-flop by the previous ADDR LD L to be transferred to a second flip-flop whose output controls the double-width MUX. This means that the value of DW H stored at the end of one DMA by ADDR LD L does not actually become effective until the beginning of the next DMA. The holding flip-flop for DW H is cleared by VERT RESET H at the start of every field. HOLD REQ H is also used to enable ADDR CNT and WRITE LB L only during DMAs. Interactions of HOLD REQ H with other signals during a DMA are further defined in Figure 4-6-19.

4.6.3 Control Chip Description

The control chip (DC012), like the timing chip, is a custom bipolar device. It accepts attribute specifications and timing signals and delivers addresses for the character generator ROM and attributes for the video output to the monitor. It also generates the HOLD REQUEST signal that halts the microprocessor and initiates DMAs to get lines of characters. Refer to the block diagram, Figure 4-6-15.

The DC012 performs three main functions.

1. Scan count generation. This involves two counters, a multiplexer to switch between the counters, double-height logic, scroll and line attribute latches, and various logic controlling switching between the two counters. This is the biggest part of the chip. It includes all scrolling, double-height logic, and feeds into the underline and hold request circuits.

2. Generation of HOLD REQUEST. This uses information from the scan counters and the scrolling logic to decide when to generate HOLD REQUEST.

3. Video modifications: dot stretching, blanking, addition of attributes to video outputs, and multiple intensity levels.

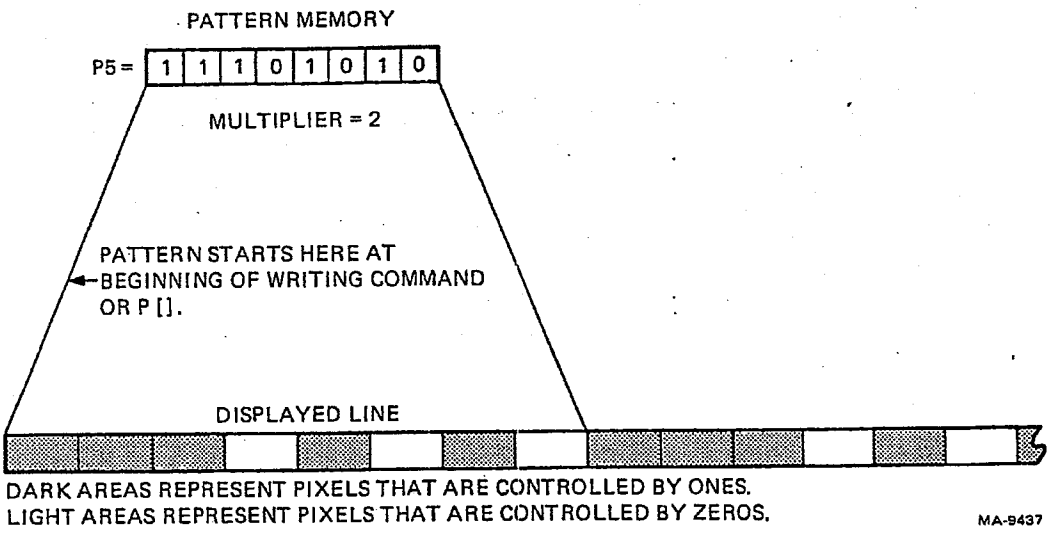


Figure 6-73 Pattern Memory and Multiplier

6.7.6 Bit Map Memory

The bit map has the following parts (Figure 6-74)

Two planes of memory. Each plane is twelve 16K X 1 DRAMs arranged in four rows of 3 DRAMs each. One RAS signal controls each row. For any bit map read, all 4 RAS signals go low at the same time to access all 12 DRAMs. (One CAS signal is common to all the DRAMs.) For a bit map write, only the RAS for the addressed row goes low. There are three write signals to drive three columns of DRAMs. Only the write signal for the addressed DRAM goes low. The intersection of one RAS signal and one write signal is only one DRAM.

Write select/disable circuit. This is a ROM that decodes address inputs to select the group of DRAMs that receive a write signal. If an address would write to a location that is not in the plane, the circuit disables all write outputs. (Such addresses occur when the graphics processor computes a graphic object that overlaps the margins of the display.)

Row/column address multiplexer. This multiplexer is controlled by the WR/RD signal and selects the source of addressing for the bit map. For most write operations, the bit map addresses come from the X and Y multiplexer, supplied by the X and Y position counters in the vector generator. For read operations, the bit map addresses come from the H and V multiplexer, supplied by the horizontal and vertical counters in the timing circuits. Each set of counters provides a total of 14 address bits. RAS TIME high selects one group of seven address signals, while RAS TIME low selects the other group.

The address lines on the multiplexers are scrambled to guarantee refreshes often enough for all the DRAMs. Each raster takes 16.7 ms, but refreshes must be less than 2 ms apart. Therefore, the address lines are arranged so that sequential addresses jump among all DRAMs at least eight times per raster. Then the vector generator address lines are scrambled in the same pattern so a given address on either side of the multiplexer always accesses the same bit. This scrambling method means the RAMs themselves do not have to reflect the H and V orientation of the counters, provided that there are enough unique addresses to cover the screen area. So a bad memory IC does not give a simple pattern on the screen, although a bad shift register line does.

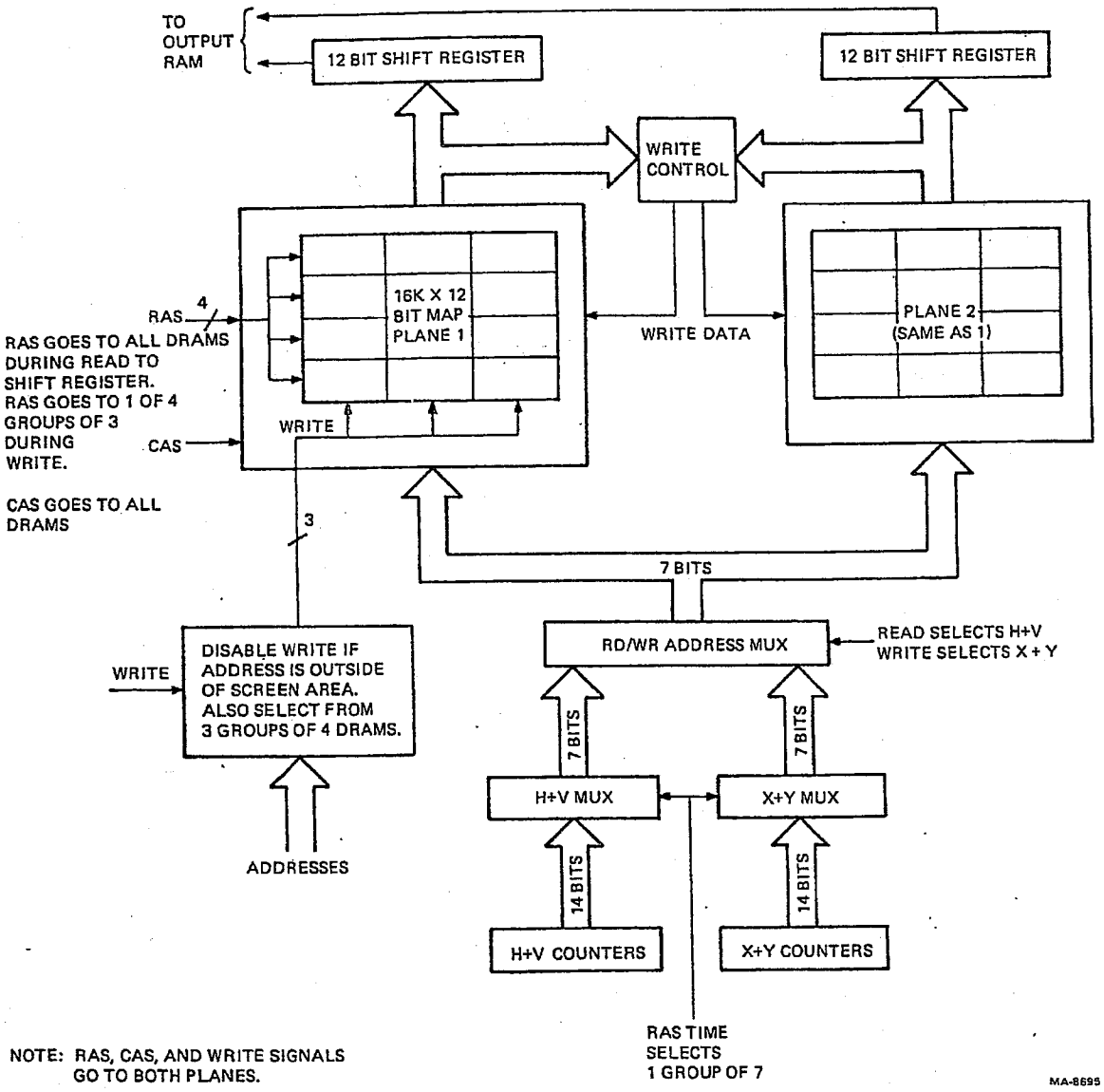


Figure 6-74 Bit Map

AX205426

Bit map output shift registers. With each bit map read cycle, each memory IC puts 1 bit on its output. The IC outputs for each plane connect directly to the inputs of three 4-bit shift registers. When LD/SHIFT is high, it strobes the inputs into the registers. The right bit in each register appears at the shift output while LD/SHIFT is high. LD/SHIFT is high for one pixel time; this means the first bit appears on the screen at LOAD time, then the other 11 bits shift onto the screen with the shift clock while LD/SHIFT is low.

6.7.7 Output Map

The VT125 displays color and brightness by addressing one of four preset values for each pixel on the screen. The VT125 can display each pixel on the screen with a different hue, lightness, or saturation. However, it can only use four different colors at one time. That is, any pixel can differ from its neighbors, but only four different colors can appear on the screen at one time. This is the tradeoff that the VT125 makes in its memory usage: rather than displaying many different colors at one time but only allowing changes at fixed boundaries that are larger than the pixel size (as in the VK100, which can change only at 12-pixel horizontal boundaries), the VT125 displays a limited set of colors at any one time but allows changes to occur at any boundary down to the individual pixel dimension.

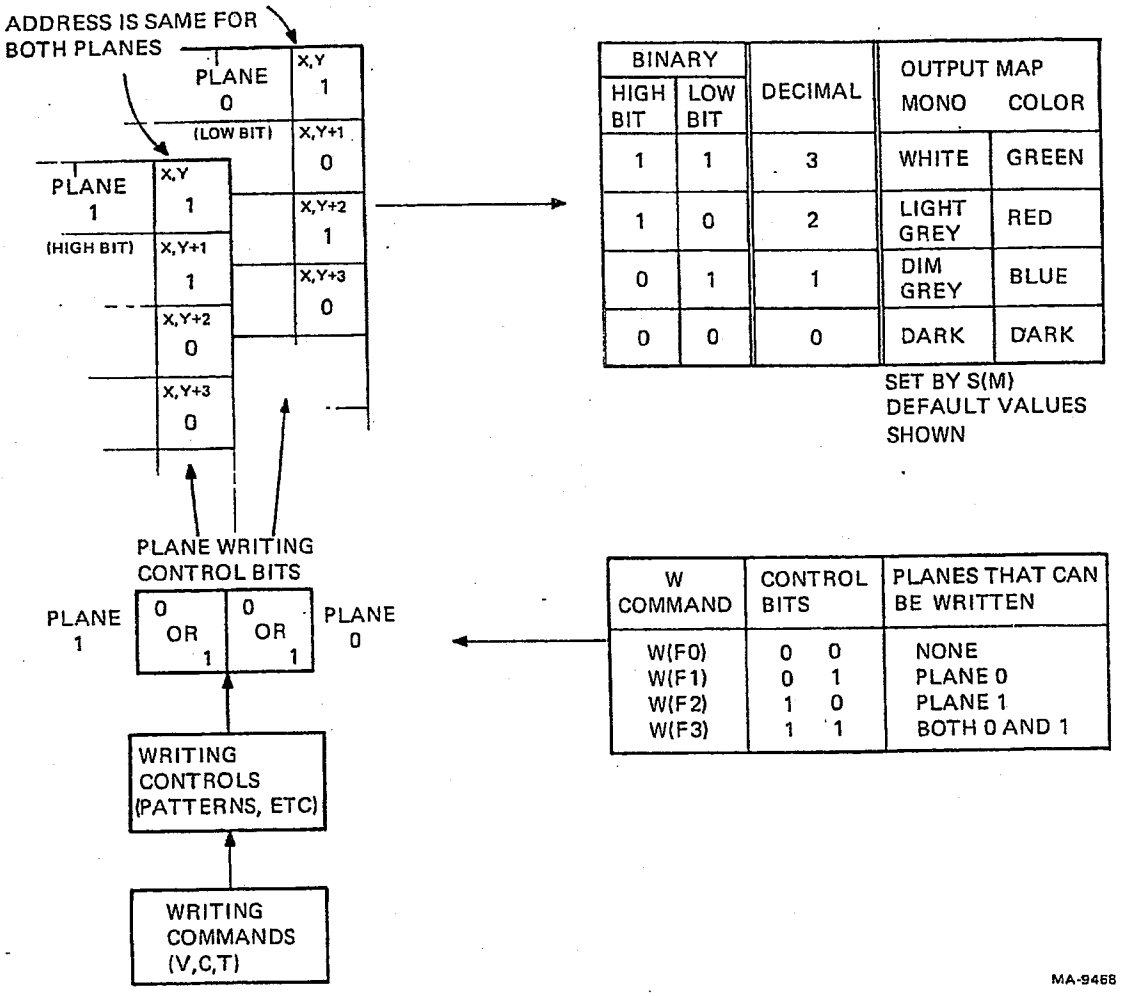
The VT125 displays color and brightness with a bit map memory and an output map. The bit map memory has the same number of addressable locations in it as the writable addresses of the screen display (768 × 256). However, for each addressable location, there are two bits of data. Think of these pairs as existing in two separate but closely connected planes of addressable locations (Figure 6-75). The pairs of bits can be written either one at a time or together. (See Writing Controls in the *VT125 User Guide.*) They represent the four numbers 0, 1, 2, and 3 when their binary values are decoded.

The four numbers are the addresses of four output map locations. Each output map location is 1 byte of a 4-byte RAM. When the graphic memory is displayed, each pixel in the bit map requests that the information in one of the output map locations be sent to the digital to analog converters (DAC). The DACs convert binary data into drive levels for cathode ray tube (CRT) gun drives. Each output map byte has 2 bits for the monochrome monitor in the VT100 part of the terminal (representing four levels of intensity on the monitor screen: dark, dim, normal, bold). Each output map byte also has 2 bits for each of the color guns in the external or alternate RGB color monitor. These bits represent four levels for each of the colors, or a total of 64 different values of hue, lightness, and saturation (HLS). (RGB is required because the National Television Standards Committee (NTSC) color standard does not provide enough bandwidth to display color changes on individual pixels.) You can set the information in each output map by using the mapping command with either RGB, letters, or HLS specifiers. (See the Screen Output Map Definition in the *VT125 User Guide.)*

6.7.8 Output Latches and DAC Converters

Each time a pixel is output from the bit map shift registers, its 2 bits (SHIFT DAT A and B) address a location in the output RAM (E58 and E46). The next SHIFT CLK strobes the data from the addressed location into latches E91 and E94. The data stays in the latch while the RAM is addressed by the next pair of data bits. The latch provides a stable signal to drive the digital to analog converters (DACs). The DACs are open collector inverters that provide paths to ground resistors in the base circuits of the video drive transistors.

Using the green output as an example, reducing the voltage on Q4's base causes more current to pass through Q4 and R77. R77 is the output load resistor; as more current passes through R77, the voltage across it increases. A CRT connected to that voltage gets brighter as the voltage increases. One way to reduce Q4's base voltage is to connect a resistor from the base to ground. The added current through R75 causes a voltage drop at the base. The DAC has two different resistors connected in parallel between the base and common. These resistors are in series with switches (the inverter output transistors) that can disconnect the resistors, or connect one or both resistors, to common. The resistors have different values, so there are four possible voltages at Q4's base. Two bits from the output RAM are inputs to the two inverters (E100) for each color plus the monochrome output.



BINARY HIGH BIT	BINARY LOW BIT	DECIMAL	OUTPUT MAP MONO	OUTPUT MAP COLOR
1	1	3	WHITE	GREEN
1	0	2	LIGHT GREY	RED
0	1	1	DIM GREY	BLUE
0	0	0	DARK	DARK

SET BY S(M)
DEFAULT VALUES SHOWN

W COMMAND	CONTROL BITS	PLANES THAT CAN BE WRITTEN
W(F0)	0 0	NONE
W(F1)	0 1	PLANE 0
W(F2)	1 0	PLANE 1
W(F3)	1 1	BOTH 0 AND 1

Figure 6-75 Bit Map Planes and the Output Map

AX205428